DESIGN OF OPTIMAL NANOSCALE CHANNEL DIMENSIONS OF FINFET BASED ON CONSTITUENT SEMICONDUCTOR MATERIALS

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We hereby declare that we have checked this thesis and in our opinion, this thesis is adequate in terms of scope and quality for the award of the degree of Master of Science.

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I hereby declare that the work in this thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at Universiti Malaysia Pahang or any other institutions.

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Thesis submitted in fulfilment of the requirements
for the award of the degree of
Master of Science

Faculty of Engineering Technology
UNIVERSITI MALAYSIA PAHANG

MAY 2019

ACKNOWLEDGMENTS

In the name of God, the Merciful praise is to God and prayers and peace on our master and our beloved Muhammad the Messenger of Allah (may Allah bless him and grant him peace) and his honourable companions and those who followed for him. Thanks to God for his grace these studies have been conducted successfully. I would like to express my appreciation and special thanks to my supervisors Dr. Waheb Abdul Jabbar Al-Areeqi, my co-supervisor, Dr. Hadi Bin Manap, and my ex-supervisor Dr. Yasir Hashim. They have always been happy and willing to help me the and direct me to the outcome of the thesis. I am grateful to Universiti Malaysia Pahang (UMP). Thanks also for the FTeK staff for their help.Finally, my regards and blessings go to my family. Words cannot express my gratitude to my parents for all the sacrifices made on my behalf. Special thanks to my wives who sacrificed in order to reach my goal. I would also like to thank all my friends who supported me and encouraged me to pursue my goal. Thank you all and God bless.

ABSTRAK

Aplikasi Nanoelectronic telah mendapat manfaat yang sangat besar daripada kemajuan besar dalam industri teknologi Nano yang baru muncul. Penurunan nilai yang besar dari dimensi transistor telah membolehkan penempatan lebih dari 100 juta transistor pada satu cip sekali gus mengurangkan fungsi peningkatan kos dan prestasi litar bersepadu (IC) yang dipertingkatkan. Walau bagaimanapun, kajian untuk mengurangken saiz transistor konvensional aken menjadi sanjat mencabar kerana kebocoran elektrostatik dan isu fabrikasi lain. Fin Field Effect Transistor (FinFET) menunjukkan potensi besar dalam penskalaan saiz dan pembuatan sebagai calon yang menjanjikan teknologi nano-oksida-semikonduktor (CMOS) pelengkap nanoscale. Struktur FinFET menyediakan kawalan elektrik yang lebih baik ke atas konduksi saluran dengan itu ia telah menarik minat yang luas dari para penyelidik dalam kedua-dua akademik dan industri. Walau bagaimanapun ,ianya secara agresif menurunkan dimensi saluran terutamanya panjang saluran akan menurunkan prestasi keseluruhan akibat kesan saluran pendek yang merugikan (SCEs). Tujuan kajian ini adalah untuk mengkaji dan menganalisis ciri-ciri elektrik pelbagai jenis transistor FinFET (Si GaAs Ge dan InAs) berdasarkan dimensi saluran untuk mengenal pasti had pengukuran fizikal optimum untuk prestasi transistor terbaik. Kajian komparatif berasaskan simulasi TIGA (3) parameter berubah-ubah: lebar panjang dan ketebalan oksida saluran dijalankan. Kesan mengubah dimensi saluran pada prestasi setiap jenis FinFET dinilai berdasarkan EMPAT (4) ciri elektrik iaitu; (i) Nisbah I_{ON} / I_{OFF} (ii) Tegasan Ambang Swing (SS) (V_T) dan Pengurangan Barrier-induced Drain (DIBL). Alat simulasi MuGFET yang terkenal untuk struktur FET pelbagai pintu gerbang nano digunakan untuk menjalankan simulasi percubaan di bawah syarat-syarat yang dipertimbangkan. Dimensi saluran optimum untuk prestasi terbaik dari semua jenis FinFET yang dipertimbangkan telah dicapai pada faktor skala minimum K = 0.125. Selain itu Si-FinFET mengatasi GaAs-FinFET dan kedua-duanya mengekalkan prestasi unggul dari segi nisbah I_{ON} / I_{OFF} dan nilai SS berbanding dengan dua jenis FinFET yang lain. Sebaliknya prestasi Ge-FinFET telah direndahkan dan mencapai nisbah I_{ON} / I_{OFF} paling rendah manakala ciri-ciri terburuk dari segi nilai SS (94 mV / dec) telah berlaku pada InAs-FinFET. Hasil penyelidikan menyumbang ke arah menganalisa had skala dan dimensi saluran penurunan tahap FinFET sebagai pengganti berpotensi untuk transistor planar dan memahaminya lagi prestasi mereka untuk mengurangkan kebocoran semasa dan masalah SCE lain.

ABSTRACT

Nano-electronic applications have benefited enormously from the great advancement in the emerging Nano-technology industry. The tremendous downscaling of the transistors' dimensions has enabled the placement of over 100 million transistors on a single chip thus reduced cost, increased functionality and enhanced performance of integrated circuits (ICs). However, reducing size of the conventional planar transistors would be exceptionally challenging due to leakages electrostatics and other fabrication issues. Fin Field Effect Transistor (FinFET) shows a great potential in scalability and manufacturability as a promising candidate in nanoscale complementary metal-oxide-semiconductor (CMOS) technologies. The structure of FinFET provides superior electrical control over the channel conduction, thus it has attracted widespread interest from researchers in both academia and industry. However, aggressively scaling down of channel dimensions, mainly the channel length, will degrade the overall performance due to detrimental short channel effects (SCEs). The aim of this study is to design optimal Nano-dimensional channel of FinFET based on electrical characteristics and semiconductor material (Si GaAs Ge and InAs) to overcome dimensions shrunk down issues and ensure the best performance of FinFETs. This was achieved by proposing a new scaling factor, *K*, to simultaneously shrinking the physical scaling limits of channel dimensions for various FinFETs without degrading their performance. A simulation-based comprehensive comparative study depending on FOUR (4) variable parameters: length, width and oxide thickness of channel in addition to scaling factor were carried out. The impact of changing channel dimensions on the performance of each type of FinFETs was evaluated base on FOUR (4) electrical characteristics namely; (i) I_{ON}/I_{OFF} ratio (ii) Subthreshold Swing (SS), (iii) Threshold voltage (V_T), and (iv) Drain-induced barrier lowering (DIBL). The well-known MuGFET simulation tool for nano-scale multi-gate FET structure is utilized to conduct experimental simulations under the considered conditions. The obtained simulation results showed that the optimal channel dimensions for best performance of all considered FinFETs types were achieved at a minimal scaling factor K = 0.125 with 5 nm length, 2.5 nm width and 0.625 nm oxide thickness of channel. Furthermore, Si-FinFET achieved the highest I_{ON}/I_{OFF} ratio (up to 2.12×10^8) and outperformed GaAs-FinFET, and both maintained a superior performance in terms of I_{ON}/I_{OFF} ratio and SS value compared to the other two types of FinFETs. In contrast, the Ge-FinFET performance was degraded and reached the lowest I_{ON}/I_{OFF} ratio (2.29×10^5), whereas the worst characteristics in terms of SS value (94 mV/dec) occurred with InAs-FinFET. The obtained results introduced new limits with enhancing FinFETs performance in terms of the investigated characteristics. The outcomes of this research contribute towards new channel nano scaling limits of FinFETs as potential successors to planar transistors in nanoscale devices and nanotechnology applications, and further analysing the electrical characteristics of FinFETs with reducing leakage current and overcoming SCEs.

TABLE OF CONTENT

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS

D	Drain
DIBL	Drain induced barrier lowering
I	current
I_d	Drain current
I_{OFF}	OFF Current
I_{ON}	ON current
K	Scaling factor
K_B	Boltzmann's coefficient
L	Length of the channel
Q	Electron charge
R_{OUT}	Output resistance
S	Source
SS	Subthreshold Swing
T	Temperature
T_{OX}	Oxide thickness
V	Voltage
V_d	Drain voltage
V_{DD}	Drain DC voltage source
V_{DS}	Drain to source voltage
V_{GS}	Gate to source voltage
V_T	Threshold voltage
W	Width of the channel

LIST OF ABBREVIATIONS

CPU	Unit processing of the central
DELTA	Depleted lean channel transistor
FDSOI	Full-Depleted Silicon
FDSoI	Depleted Silicon On Insulator
FET	Field Effect Transistor
FinFET	Fin-shaped field effect transistor
GAA	Gate all around
GaAs	Gallium Arsenide
GaN	Gallium Nitride
Ge	Germanium
GIDL	Gate-induced drain leakage
IC	Integrated Circuits
InAs	Indium Arsenide
JFETs	Junction field effect transistor
MOSFET	Metal-Oxide-field-effect transistor
MuGFET	Multi-Gate-Field Effect Transistor
NW	Nanowire
PDSOI	Partially-Depleted Silicon
Rsd	Resistance source drain
SCE	Short channel effect
Si	Silicon
SiC	Silicon Carbide
SiNWT	Silicon nanowire transistor
SOI	Silicon on insulator
VLST-TSA	Technology Systems and Application

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